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(54) Signal processing apparatus.

(57) A signal processing apparatus is disclosed which includes a low speed ROM (9) for storing a plurality of signal procedures, a high speed RAM (4) used by a digital signal processor DSP (5), a control processor CPU (8) for transferring a signal procedures from the low speed ROM (9) to the high speed RAM (4), a digital signal processor DSP (5) for processing the signal procedures loaded in the high speed RAM (4). Accordingly, a signal processing apparatus of the present invention is constructed with low cost memory, then reduces manufacturing cost of the apparatus.

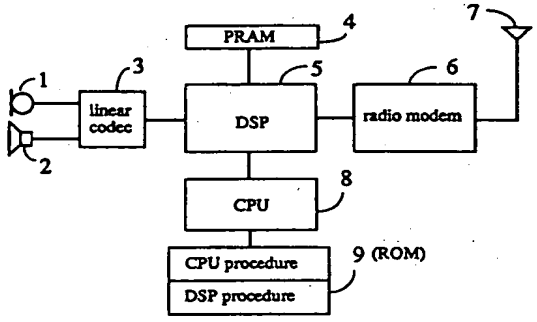

FIG. 1

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The invention relates to a signal processing apparatus which is applicable to a radio communication apparatus.

FIG. 4 shows a block diagram of a conventional signal processing apparatus as applied to a radio communication system. In FIG. 4, an analog output voice signal from a microphone 1 is converted to a digital signal in a linear codec 3. A digital signal processor (DSP) 5 executes a coding process, a data compression process and an error correction process according to the instruction stored in a high speed PROM 24 and outputs coded data to a radio modem 6. The radio modem 6 modulates the coding data received from DSP 5 according to the instruction from a control processor 8 which controls the devices in the signal processing apparatus and transmits the modulated radio signal to the base station (not shown) via an antenna 7.

In the case of receiving the radio signal from the base station, the radio signal is input to the radio modem 6 via the antenna 7. The radio modem 6 demodulates the modulated signal and sends it to the DSP 5. The DSP 5 decodes the coded signal according to the instruction procedure stored in the high speed PROM 24 and sends the decoded digital signal to the linear codec 3. The linear codec 3 converts the digital signal to an analog signal and sends the analog signal to a speaker 2.

FIG. 5 shows a block diagram of a second conventional signal processing apparatus which is also applied to radio communication systems. FIG. 5 is different from the FIG. 4 in that the high speed PROM 24 in FIG. 5 includes a plurality of different kinds of procedures. The DSP 5 selects one of the procedures stored in the high speed PROM 24 and controls the processes according to the selected procedure. In FIG. 5, the operation of the signal processing apparatus is otherwise the same as that of the FIG. 4. Therefore further detailed description is omitted.

As discussed above, this apparatus is designed so that the DSP 5 processes a plurality of procedures stored in the PROM 24. Since the DSP 5 operates at a high speed, the PROM 24 must also be operated at a high speed. But, the cost of the PROM 24 is very expensive because it must operate at very high speed. If the PROM 24 includes many procedures which are processed in the DSP 5, the cost will increase further.

Therefore, it is a primary object of the present invention to provide a signal processing apparatus in which a plurality of signal procedures are stored in a low cost and low speed ROM.

It is further object of the present invention to provide a signal processing apparatus in which a control processor CPU loads a plurality of signal procedures from the low speed ROM to the high speed RAM, and a digital signal processor DSP processes the signal procedures loaded in the high speed RAM.

It is still further object of the invention to provides a signal processing apparatus using a low cost memory.

A signal processing apparatus according to the present invention includes a low speed ROM for storing a plurality of signal procedures, a high speed RAM used by a digital signal processor, a control processor CPU for transferring a signal procedures from the low speed ROM to the high speed RAM and a digital signal processor DSP for processing the signal procedures loaded in the high speed RAM.

FIG. 1 is a block diagram of a first embodiment of a signal processing apparatus of the present invention.

FIG. 2 is a block diagram of a second embodiment of a signal processing apparatus of the present invention.

FIG. 3 is a block diagram of a third embodiment of a signal processing apparatus of the present invention.

FIG. 4 is a block diagram of a first conventional signal processing apparatus.

FIG. 5 is a block diagram of a second conventional signal processing apparatus.

The operation of the first embodiment is explained hereinafter with reference to FIG. 1 . An analog output voice signal from the microphone 1 is converted to a digital signal in a linear codec 3. A digital signal processor (DSP) 5 executes a number of different kinds of signal processes according to the instruction procedures stored in a programmable random access memory (PRAM) 4 and outputs the coded signal to a radio modem 6. The radio modem 6 modulates the coded data received from DSP 5 and transmits the modulated radio signal to the base station (not shown) via the antenna 7.

The received radio signal is input to the radio modem 6 via the antenna 7. The radio modem 6 demodulates the radio signal to derive the demodulated digital signal. The DSP 5 executes different kinds of signal processes according to the instruction procedures stored in PRAM 4 and outputs the decoded signal to the linear codec 3. The linear codec 3 converts the digital signal to an analog signal and sends it to the speaker 2. The speaker 2 converts the analog signal to voice output.

In FIG. 1, high speed PRAM 4 is a programmable random access memory which is used for DSP 5. A low speed ROM 9 stores a plurality of instruction procedures used in DSP 5 as well as the instruction procedures used in a control processor CPU 8. Control processor CPU 8 transfers the

instruction procedures from the low speed ROM 9 to the high speed PRAM 4 through DSP 5. The digital signal processor DSP 5 executes the instruction procedures stored in the high speed PRAM 4 which has been transferred from the ROM 9. In FIG. 1, the same reference numbers as used in the FIG. 4 refer to the same components or the corresponding components. Accordingly the detailed explanation of such components is omitted in connection with those having the same number.

In the usual operation of the digital signal processor DSP 5, each procedure is not processed at the same time but one of the procedures is selected from a plurality of the procedures. Then the digital signal processor DSP 5 executes the selected one of the procedures. Therefore, in the present invention, instead of storing the procedures in the high speed PROM 24 as shown in the conventional art of FIG. 5, the procedures are stored in the low speed ROM 9. The procedures loaded from the ROM 9 into the high speed PRAM 4 when needed by the CPU 8 using interprocessor communication between the CPU 8 and the digital signal processor DSP 5. The CPU 8 lets the digital signal processor DSP 5 start after verifying the complete loading of the procedures into the high speed PRAM 4 from the ROM 9.

In the above embodiment, the signal procedures are independent from other signal procedures. In this case, the procedure for processing the signal must be substituted entirely if another signal procedure is selected. Therefore it is necessary to transfer a large amount of data from the ROM 9 to PRAM 4. If there are some common procedures in the plurality of the signal procedures, the common procedures can be used without being substituted between the plurality of the signal procedures.

In the above embodiment, PRAM 4 is provided external to the DSP 5, but can be incorporated within DSP 5, if DSP 5 has its own internal RAM. In this case the circuit configuration can be further simplified.

In the above embodiment, voice coding procedures are described, but the present invention may be also applied to data transmission, facsimile transmission and other applications which do not use voice signals. In this case, the applicable data procedures are also stored in the ROM 9.

FIG. 2 is a block diagram of a second embodiment of a signal processing apparatus of the present invention. In FIG. 2, an analog signal is input to or output from a handset 1a which includes a microphone and speaker. A digital signal is input through a digital interface circuit 10. The digital interface circuit 10, such as an RS-232 interface, is connected to external digital devices, such as a personal computer. An analog signal such as facsimile signal is input from an analog interface 11 such as RJ-11. In the low speed ROM 9 , data transmission procedure and facsimile procedure are stored as well as voice processing procedure. A linear codec 3 converts the analog signal to a digital signal and the digital signal to an analog signal. The DSP 5 executes different kinds of signal procedures including analog procedures and digital procedures according to the signal procedures stored in the high speed PRAM 4 which are transferred from the low speed ROM 9 by the CPU 8 using interprocessor communication.

In the above embodiment, the DSP 5 processes the base band signal and may also perform part of the functions of the radio modem 6.

FIG. 3 is a block diagram of a third embodiment of a signal processing apparatus of the present invention. In this embodiment, the DSP is divided into two portions a DSP-1 indicated by number 5 and a DSP-2 indicated by number 15. The DSP-1 operates to process the base band signal. The DSP-2 operates to process the modem signal. The PRAM is also divided into two portions PRAM-1 indicated by number 4 and PRAM-2 indicated by number 14. The CPU 8 transfers the baseband procedure from the low speed ROM 9 to the high speed PRAM-1, and the DSP-1 processes the base band procedure using procedure stored in the PRAM-1. The CPU 8 also transfers the modem procedure from the low speed ROM 9 to the high speed PRAM-2, and the DSP-2 processes the modem procedure using the procedure stored in the PRAM-2.

Claims

1. A signal processing apparatus for processing digital signals, comprising:
   - a random access memory (RAM)(4, 14) for a digital signal processor (DSP)(5, 15);
   - a read only memory (ROM)(9) for storing signal procedures for use in a digital signal processor (5, 15) and a control processor (CPU)(8);
   - a control processor (8) for controlling all devices in the signal processing apparatus, and transferring the signal procedures from the ROM (9) to the RAM (4, 14);
     and
   - a digital signal processor (8) for executing the signal processing according to a plurality of signal procedures stored in the RAM (4, 14) which are transferred from the ROM (9).

2. The apparatus according to claim 1, further

comprising:

- a linear codec (3) which is connected to the input of the DSP (5, 15) and converts an analog signal into a digital signal or a digital signal into an analog signal.

3. The apparatus according to claim 1 or 2, further comprising:
   - a modem (6, 16) which is connected to the output of the DSP (5, 15) and modulates or demodulates the signal.

4. The apparatus according to any of claims 1 to 3, further comprising:
   - a digital interface (10) which is connected to the input of the DSP (5, 15) and interfaces an outgoing signal and an incoming signal.

5. The apparatus according to any of claims 1 to 4, further comprising:
   - a modem (6, 16) which is connected to the output of the DSP (5, 15) and modulates or demodulates the signal.

6. The apparatus according to any of claims 2 to 5, further comprising:
   - an analog interface (11) which is connected to the input of the linear codec (3) and interfaces the outgoing signal and the incoming signal.

7. The apparatus according to claim 6, further comprising:
   - a modem (6, 16) which is connected to the output of the DSP (5, 15) and modulates or demodulates the signal.

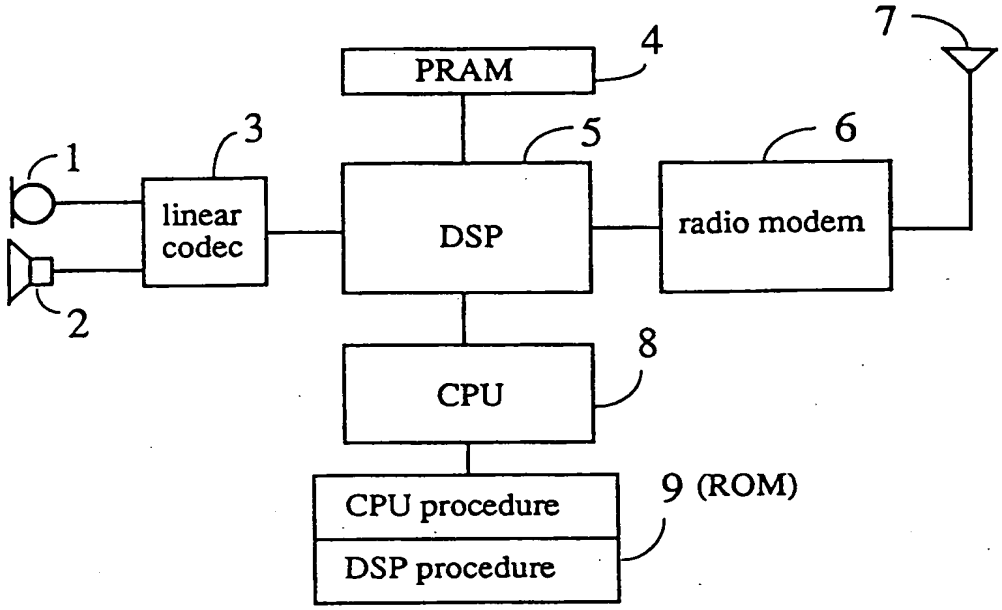
PRAM
4
7
3
5
6
1
linear codec
DSP
radio modem
2
8
CPU
9 (ROM)
CPU procedure
DSP procedure

FIG. 1

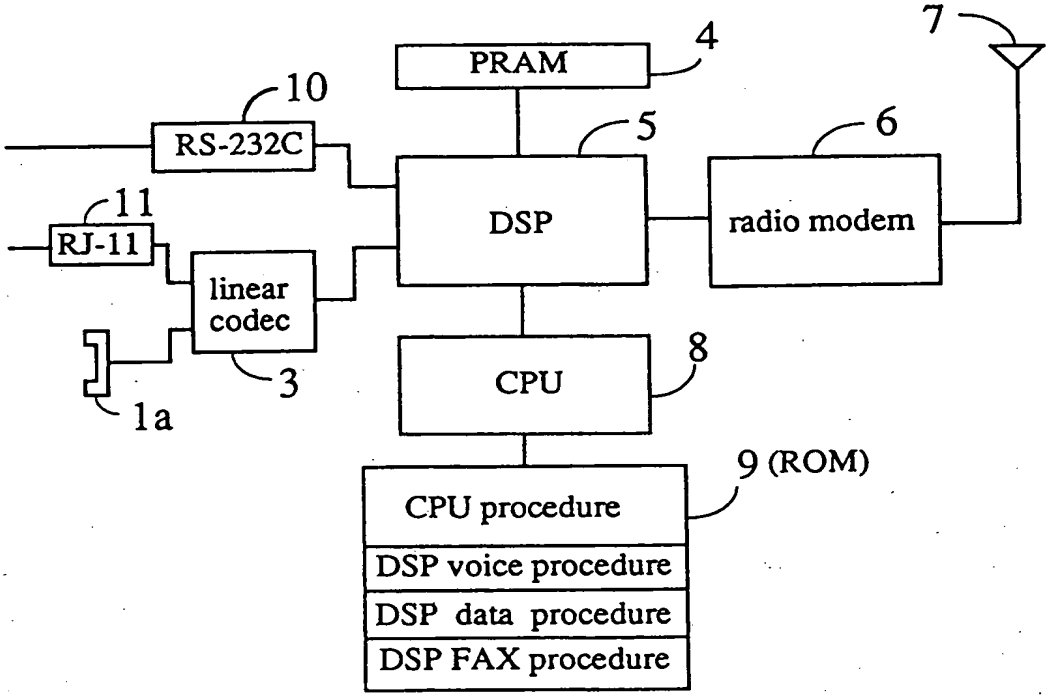
PRAM
4
7
10
5
6
RS-232C
11
RJ-11
DSP
radio modem
linear codec
3
8
CPU
1a
9 (ROM)
CPU procedure
DSP voice procedure
DSP data procedure
DSP FAX procedure

FIG. 2

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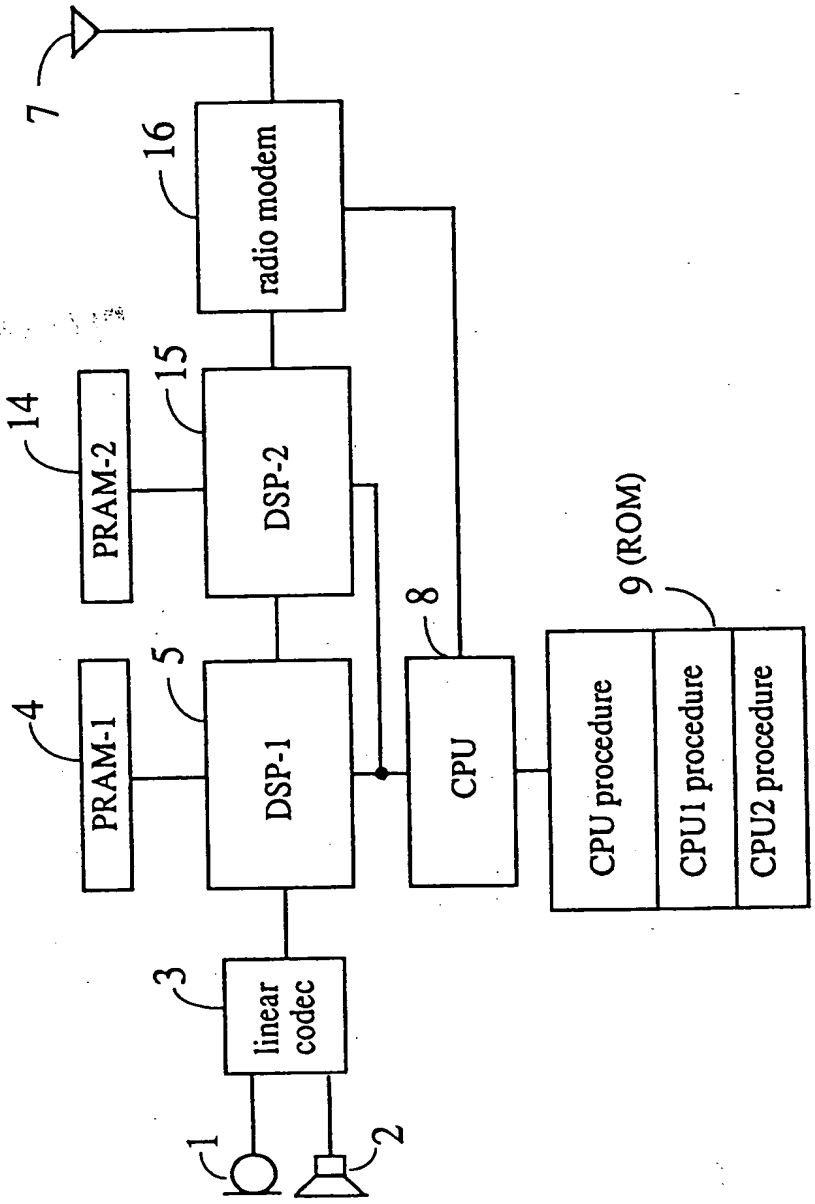
7
16
radio modem
15
DSP-2
14
PRAM-2
8
9 (ROM)
5
DSP-1
4
PRAM-1
CPU
CPU procedure
CPU1 procedure
CPU2 procedure
3
linear codec
1
2

FIG. 3

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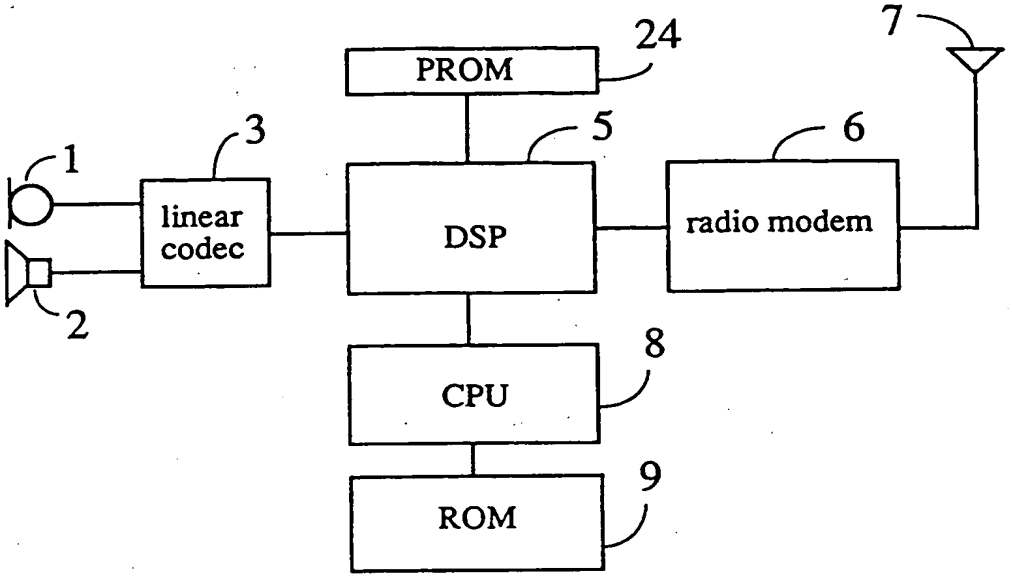

FIG. 4 (PRIOR ART)

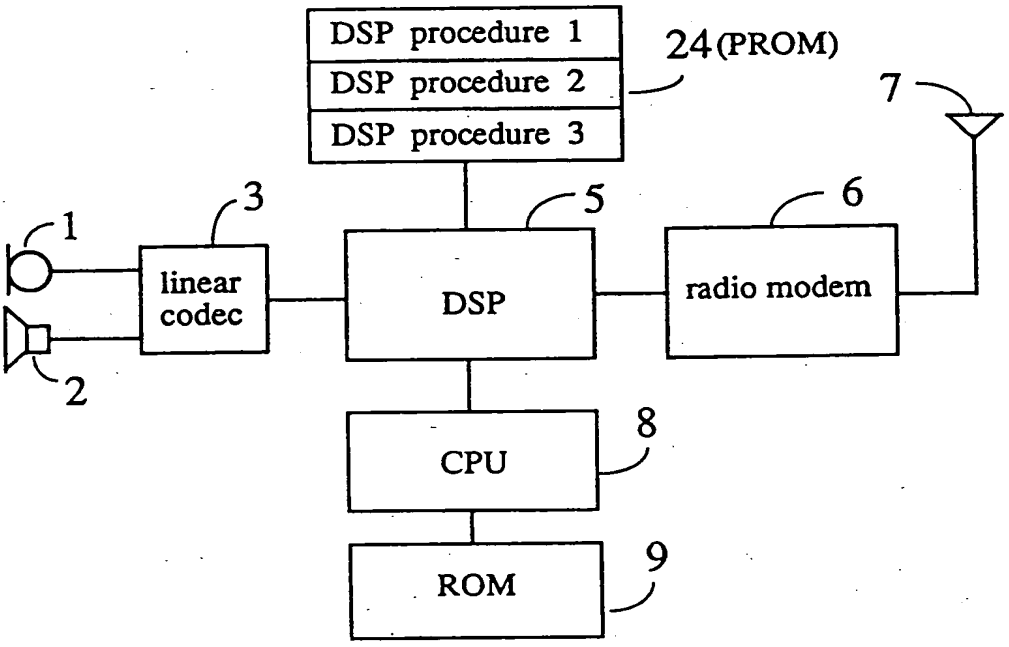

FIG. 5 (PRIOR ART)

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